The documentation and process conversion measures necessary to comply with this revision shall be completed by 17 August 2004.

INCH-POUND

MIL-PRF-19500/397H
17 June 2004
SUPERSEDING
MIL-PRF-19500/397G
1 April 2002

* PERFORMANCE SPECIFICATION SHEET

* SEMICONDUCTOR DEVICE, TRANSISTOR, PNP, SILICON,
TYPES 2N3743, 2N3743U4, 2N4930, 2N4930U4, 2N4931, AND 2N4931U4,
JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP, silicon, high-voltage transistor. Four levels of product assurance are provided for each device type as specified in MIL-PRF-19500. Two levels of product assurance for die are provided for each unencapsulated device type as specified in MIL-PRF-19500

* 1.2 Physical dimensions. See figure 1 (TO-39), figure 2 (U4), and figures 3 and 4 for JANHC and JANKC (die) dimensions.

* 1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Type	P_T (1) T_A = +25°C	P_T (2) T_{PCB} = +25°C	P_T (2) T_C = +25°C	$R_{\theta JA}$	$R_{\theta JPCB}$	$R_{\theta JC}$	V_{CBO}	V_{EBO}	V_{CEO}	I_C	T_J and T_{STG}
	W	W	W	°C/W	°C/W	°C/W	V dc	V dc	V dc	mA dc	°C
2N3743	1.0		5	175		30	300	5	300	200	-65 to +200
2N4930	1.0		5	175		30	200	5	200	200	-65 to +200
2N4931	1.0		5	175		30	250	5	250	200	-65 to +200
2N3743U4		1.0	10		175	15	300	5	300	200	-65 to +200
2N4930U4		1.0	10		175	15	200	5	200	200	-65 to +200
2N4931U4		1.0	10		175	15	250	5	250	200	-65 to +200

(1) For derating see figures 5 through 16.
(2) For thermal curves see figures 17, 18, and 19.

Comments, suggestions, or questions on this document should be addressed to: Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://www.dodssp.daps.mil.

1.4 Primary electrical characteristics at T_A= +25°C.

Limits	$\|h_{fe}\|$	h_{FE1} (1)	h_{FE4} (1)	$V_{BE(sat)2}$ (1)	$V_{CE(sat)1}$ (1)	C_{obo}
	I_C = 10 mA dc V_{CE} = 20 V dc f = 20 MHz	I_C = 0.1 mA dc V_{CE} = 10 V dc	I_C = 30 mA dc V_{CE} = 10 V dc	I_C = 30 mA dc I_B = 3 mA dc	I_C = 30 mA dc I_B = 3 mA dc	I_E = 0 V_{CB} = 20 V dc f ≥ 0.1 MHz
				V dc	V dc	pF
Min	2.0	30	50			
Max	8.0		200	1.2	1.2	15

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

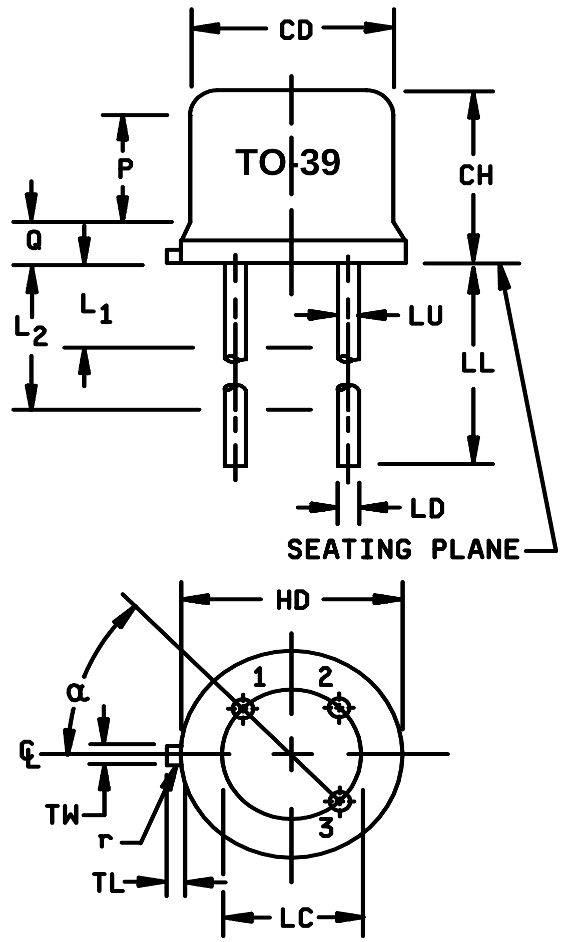
DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch or http://www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

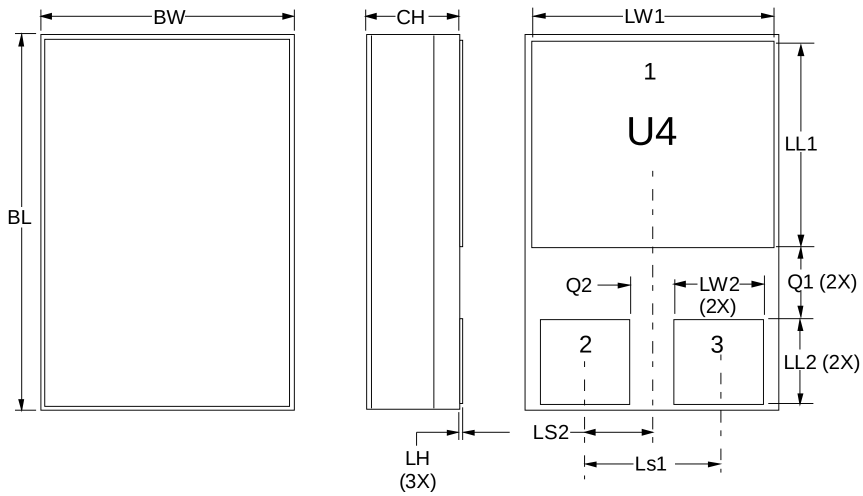
2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.12	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		7
LD	.016	.019	0.41	0.48	8,9
LL	.500	.750	12.7	19.0	
LU	.016	.019	0.41	0.48	8,9
L1		.050		1.27	8,9
L2	.250		6.35		8,9
P	.100		2.54		6
Q		.030		0.76	5
TL	.029	.045	0.74	1.14	3,4
TW	.028	.034	0.71	0.86	3, 4
r		.010		0.25	
α	45° TP		45° TP		



NOTES:
1. Dimensions are in inches.
2. Millimeter equivalents are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
7. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by the gauge and gauging procedure.
8. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
9. All three leads.
10. The collector shall be internally connected to the case.
11. Dimension r (radius) applies to both inside corners of tab.
12. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
13. Lead 1 = emitter, lead 2 = base, lead 3 = collector.

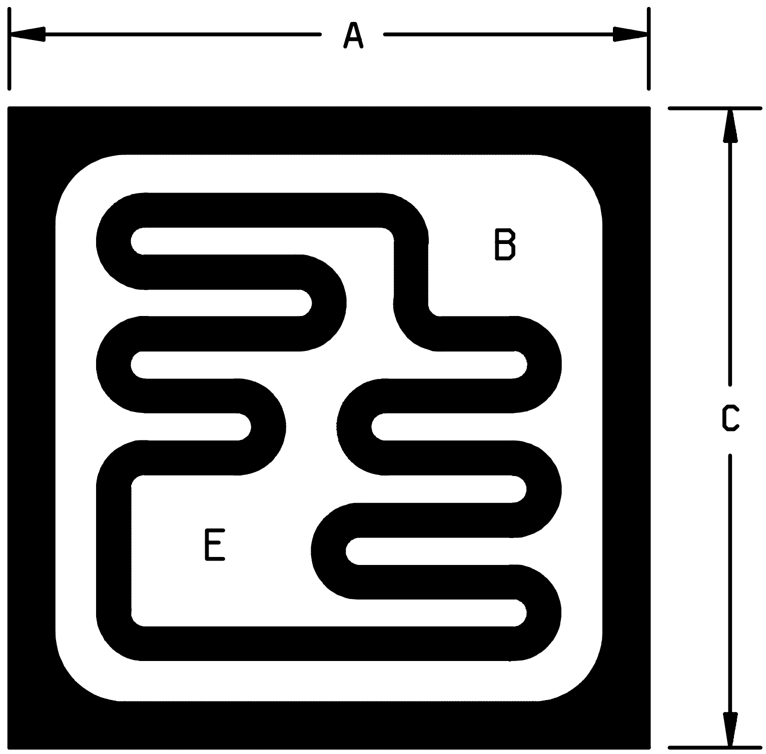
* FIGURE 1. Physical dimensions (TO-39).



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.215	.225	5.46	5.72
BW	.145	.155	3.68	3.94
CH	.049	.075	1.24	1.91
LH	-	.005	-	0.127
LW1	.135	.145	3.43	3.68
LW2	.047	.057	1.19	1.45
LL1	.115	.125	2.92	3.18
LL2	.045	.055	1.14	1.40
LS1	.070	.095	1.78	2.41
LS2	.038	.048	.965	1.22
Q1	.045	.070	1.14	1.78
Q2	.025	.035	0.635	0.89
Terminal	BIPOLAR			
1	Collector			
2	Base			
3	Emitter			

NOTES:
1. Dimensions are in inches.
2. Millimeter equivalents are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

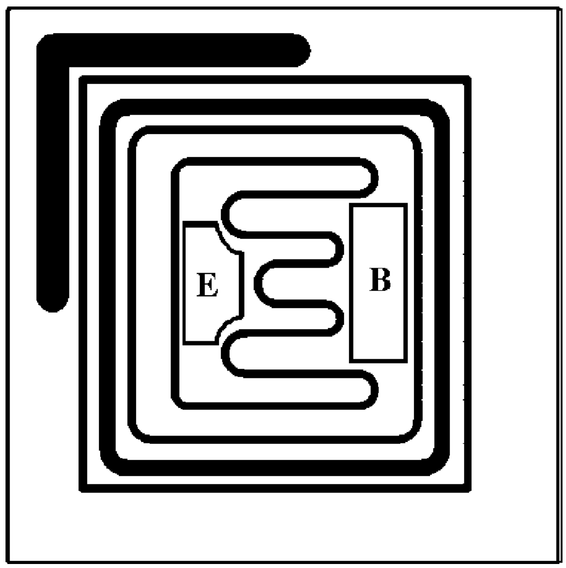
* FIGURE 2. Physical dimensions and configuration (U4).



Letter	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.041	.041	1.04	1.04
C	.041	.041	1.04	1.04

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. The physical characteristics of the die are:
   Thickness: .006 inch (0.15 mm) to .012 inch (0.30 mm).
   Top metal: Aluminum 17,500 Å minimum, 20,000 Å nominal.
   Back metal: Gold 2,500 Å minimum, 3,000 Å nominal.
   Back side: Collector.
   Bonding pad: B = .004 inch (0.10 mm) x .005 inch (0.13 mm).
   E = .004 inch (0.10 mm) x .0055 inch (0.14 mm).
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 3. JANHC and JANKC (A-version) die dimensions.



NOTES:
1. Chip size: 40 x 40 mils ±1 mil.
2. Chip thickness: 10 ±1.5 mil.
3. Top metal: Aluminum 15,000Å minimum, 18,000Å nominal.
4. Back metal: A. Al/Ti/Ni/Ag 12kÅ/3kÅ/7kÅ/7kÅ min., 15kÅ/5kÅ/10kÅ/10kÅ nom.
   B. Gold 2,500Å minimum, 3,000Å nominal.
   C. Eutectic Mount – No Gold.
5. Backside: Collector
6. Bonding pad: B = 6 x 8 mils, E = 6 x 4 mils.

* FIGURE 4. JANHC and JANKC (B-version) die dimensions.

3. REQUIREMENTS

* 3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list before contract award (see 4.2 and 6.3).

* 3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

$R_{\theta JSP}$...................... Thermal resistance junction to solder pads (adhesive mount to PCB).

* 3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (TO-39), figure 2, and figures 3 and 4 for JANHC and JANKC (die) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4 and table I.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.

* 3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

* 4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
3c	Thermal impedance, method 3131 of MIL-STD-750.	Thermal impedance, method 3131 of MIL-STD-750.
9	I_{CBO1}	Not applicable
11	I_{CBO1} and h_{FE4} ΔI_{CBO} = 100 percent of initial value or 50 nA dc, whichever is greater	I_{CBO1} and h_{FE4}
12	See 4.3.1 240 hours minimum	See 4.3.1
13	Subgroups 2 and 3 of table I herein; ΔI_{CBO1} = 100 percent of initial value or 50 nA dc, whichever is greater; $\Delta h_{FE4} = \pm 15$ percent	Subgroup 2 of table I herein; ΔI_{CBO1} = 100 percent of initial value or 50 nA dc, whichever is greater; $\Delta h_{FE4} = \pm 20$ percent
14	Required	Required

* 4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 V dc, T_A = 25°C + 5°C. Power shall be applied to the device to achieve the required junction temperature, T_J = +135°C minimum using a minimum power dissipation = 75 percent of max P_T as defined in 1.3. NOTE: No heat sink or forced air cooling on the devices shall be permitted. Power burn-in conditions for "U4" suffix devices are identical to their corresponding non suffix devices.

4.3.2 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500, “Discrete Semiconductor Die/Chip Lot Acceptance”. Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

* 4.3.3 Thermal impedance ($Z_{\theta JX}$ measurements). The $Z_{\theta JX}$ measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). The $Z_{\theta JX}$ limit used in screen 3c of 4.3 and subgroup 2 of table I shall comply with the thermal impedance graph on figures 17 through 19 (less than or equal to the curve value at the same t_H time) or shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein. Electrical measurements (end-points) shall be in accordance with the applicable inspections of table I, subgroup 2 herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in VIa (JANS) and 4.4.2.1 herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with table I, subgroup 2 herein.

* 4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B4	1037	V_{CE} = 30 V dc, 2,000 cycles.
B5	1027	(NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample). V_{CB} = 10 V dc; $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). Option 1: 96 hours minimum, sample size in accordance with table VIa of MIL-PRF-19500, adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hours, sample size = 45, c = 0; adjust T_A or P_D to achieve T_J = +225°C minimum.
B6	3131	$R_{\theta JA}$ for TO-5, UA, and UB. $R_{\theta JC}$ for U4.

* 4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action.

Step	Method	Condition
1	1039	Steady-state life: Test condition B, 1,000 hours minimum, V_{CB} = 10 V dc, power shall be applied to achieve T_J = +175°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0.
2	1039	HTRB: Test condition A, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), T_A = +200°C. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Must be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

* 4.4.3 Group C inspection, Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500 and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.3.1 Group C inspection, table VII (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E; (Not applicable for U4 devices).
C6	1026	V_{CB} = 10 to 30 V dc; T_J = + 175°C minimum. No heat sink or forced-air cooling on the devices shall be permitted.

4.4.3.2 Group C inspection, table VII (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E; (Not applicable for U4 devices).
C5	3131	See 4.4.5 $R_{\theta JA}$ for TO-5. $R_{\theta JC}$ for U4.
C6		Not applicable

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests for conformance inspection. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table IX of MIL-PRF-19500 and as specified herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

* 4.4.5 Thermal resistance. Thermal resistance measurements shall be conducted in accordance with method 3131 of MIL-STD-750.

a. I_M measurement.. 10 mA.

b. V_{CE} measurement voltage (same as V_H)................................... 25 V dc.

c. I_H collector heating current... 0.2 A dc.

d. V_H collector-emitter heating voltage .... 25 V dc.

e. t_H heating time .... 1 second minimum.

f. t_{MD} measurement delay time .... 50 µs maximum.

g. t_{SW} sampling window time .... 10 µs maximum.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical examination 3/	2071	n = 45 devices, c = 0				
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvent 3/ 4/ 5/	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal 4/	1071	n = 22 devices, c = 0				
Fine leak Gross leak						
Electrical measurements 4/		Table I, subgroup 2				
Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hrs or T_A = +300°C at t = 2 hrs, n = 11 wires, c = 0				
Decap internal visual (design verification)	2075	n = 4 devices, c = 0				
Subgroup 2						
* Thermal Impedance	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
Breakdown voltage, collector to base	3001	Bias condition D, I_C = 100 µA dc	$V_{(BR)CBO}$			
2N3743, U4 2N4930, U4 2N4931, U4				300 200 250		V dc V dc V dc
Breakdown voltage, collector to emitter	3011	Pulsed (see 4.5.1), bias condition D, I_C = 1.0 mA dc	$V_{(BR)CEO}$			
2N3743, U4 2N4930, U4 2N4931, U4				300 200 250		V dc V dc V dc
Breakdown voltage, emitter to base	3026	Bias condition D, I_E = 100 µA dc	$V_{(BR)EBO}$	5		V dc
Collector to base cutoff current	3036	Bias condition D, I_E = 0	I_{CBO1}		250	nA
2N3743, U4 2N4930, U4 2N4931, U4		V_{CB} = 250 V dc V_{CB} = 150 V dc V_{CB} = 200 V dc				
Emitter to base cutoff current	3061	Bias condition D, V_{EB} = 4 V dc	I_{EBO}		150	nA dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued.						
Forward current transfer ratio	3076	Pulsed (see 4.5.1), I_C = 0.1 mA dc, V_{CE} = 10 V dc	h_{FE1}	30		
Forward current transfer ratio	3076	Pulsed (see 4.5.1), I_C = 1.0 mA dc, V_{CE} = 10 V dc	h_{FE2}	40		
Forward current transfer ratio	3076	Pulsed (see 4.5.1), I_C = 10 mA dc, V_{CE} = 10 V dc	h_{FE3}	40		
Forward current transfer ratio	3076	Pulsed (see 4.5.1), I_C = 30 mA dc, V_{CE} = 10 V dc	h_{FE4}	50	200	
Forward current transfer ratio	3076	Pulsed (see 4.5.1), I_C = 50 mA dc, V_{CE} = 20 V dc	h_{FE5}	30		
Collector to emitter voltage (saturated)	3071	Pulsed (see 4.5.1), I_C = 30 mA dc, I_B = 3 mA dc	$V_{CE(sat)1}$		1.2	V dc
Collector to emitter voltage (saturated)	3071	Pulsed (see 4.5.1), I_C = 10 mA dc, I_B = 1 mA dc	$V_{CE(sat)2}$		1.0	V dc
Base emitter voltage (saturated)	3066	Test condition A, I_C = 10 mA dc, I_B = 1 mA dc, pulsed (see 4.5.1)	$V_{BE(sat)1}$		1.0	V dc
Base emitter voltage (saturated)	3066	Test condition A, I_C = 30 mA dc, I_B = 3 mA dc, pulsed (see 4.5.1)	$V_{BE(sat)2}$		1.2	V dc
Subgroup 3						
High-temperature operation:		T_A = +150°C				
Collector to base cutoff current	3036	Bias condition D	I_{CBO2}		5	μA dc
2N3743, U4 2N4930, U4 2N4931, U4		V_{CB} = 250 V dc V_{CB} = 150 V dc V_{CB} = 200 V dc				
Low-temperature operation:		T_A = -55°C				
Forward current transfer ratio	3076	Pulsed (see 4.5.1), I_C = 30 mA dc, V_{CE} = 10 V dc	h_{FE6}	25		
Subgroup 4						
Open circuit (output capacitance)	3236	V_{CB} = 20 V dc, I_E = 0, f ≥ 0.1 MHz	C_{obo}		15	pF
Input capacitance (output open circuited)	3240	V_{EB} = 1 V dc, I_C = 0, f ≥ 0.1 MHz	C_{ibo}		400	pF

See footnotes at end of table.

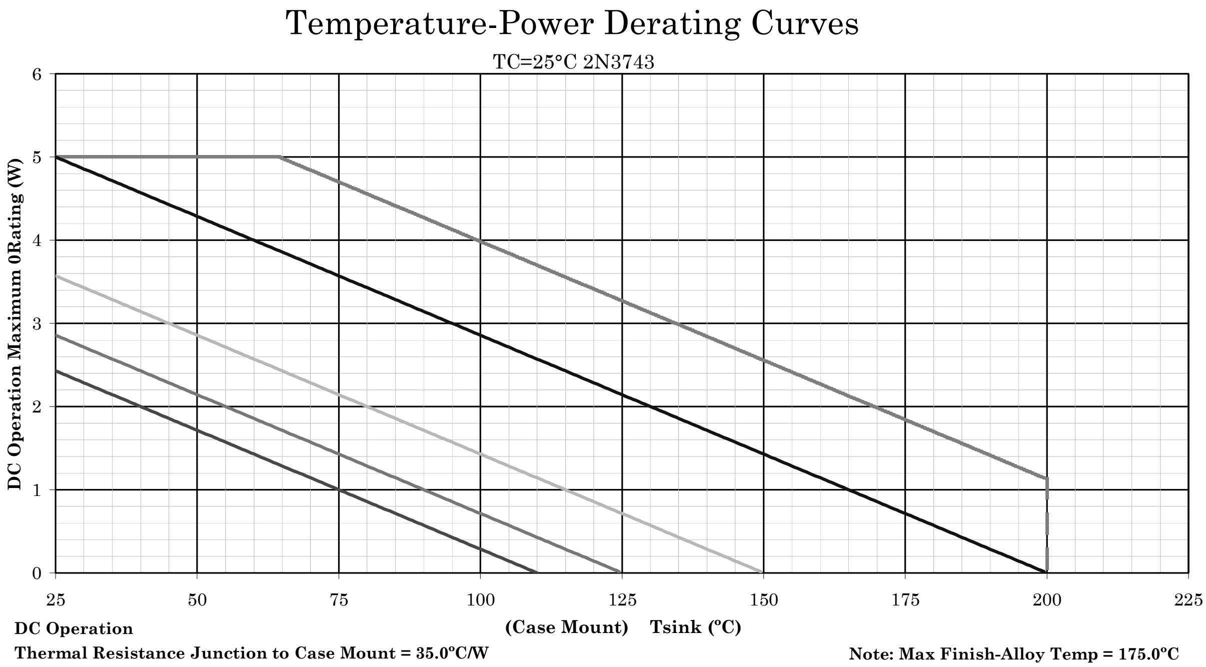
TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 4 - Continued.						
Small-signal current gain	3306	V_{CE} = 20 V dc, I_C = 10 mA dc, f = 20 MHz	$\|h_{fe}\|$	2	8	
Small-signal current gain	3206	V_{CE} = 10 V dc, I_C = 10 mA dc, f = 1 kHz	h_{fe}	30	300	
Subgroup 5						
Safe operating area (dc operation)	3051	T_C = +25°C, t ≥ 1 second, 1 cycle				
Test 1		I_C = 50 mA dc, V_{CE} = 20 V dc				
Test 2		I_C = 10 mA dc, V_{CE} = 100 V dc				
Test 3						
2N3743, U4		I_C = 3.3 mA dc, V_{CE} = 300 V dc				
2N4930, U4		I_C = 5 mA dc, V_{CE} = 200 V dc				
2N4931, U4		I_C = 4 mA dc, V_{CE} = 250 V dc				
Electrical measurements		See table I, subgroup 2 herein				

1/ For sampling plan, see MIL-PRF-19500.
2/ For resubmission of failed subgroup 1, double the sample size of the failed test or sequence of tests.
3/ Separate samples may be used.
4/ Not required for JANS.
5/ Not required for laser marked devices.

* TABLE II. Group E inspection (all quality levels) – for qualification and re-qualification only.

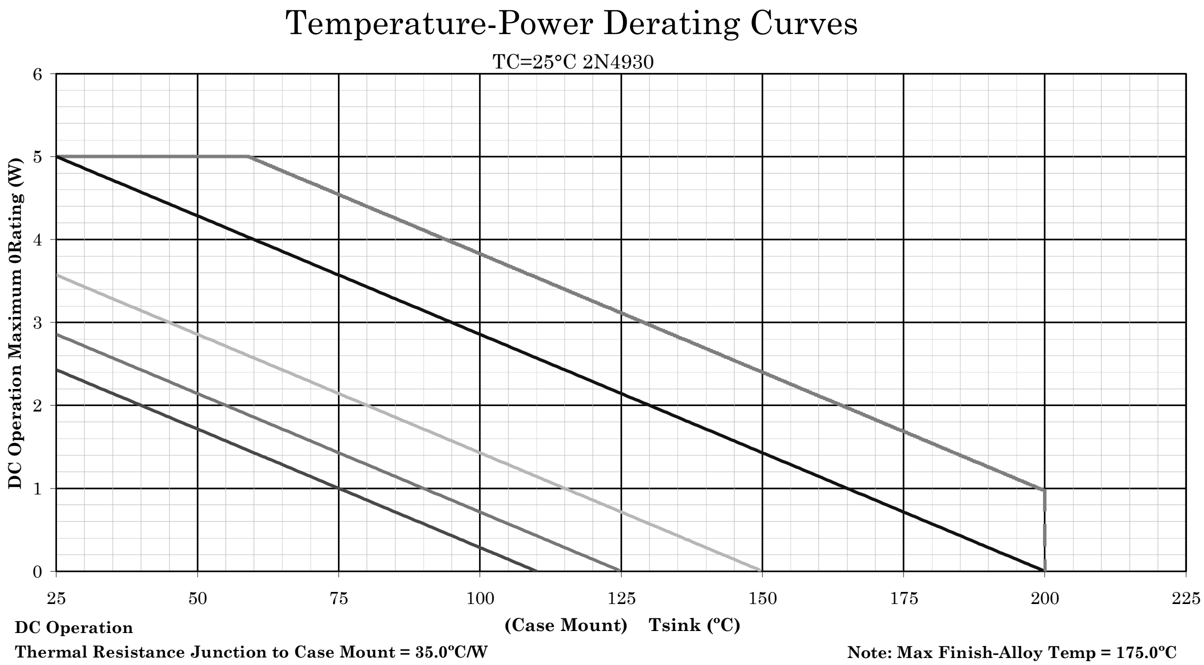
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal			
Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	V_{CB} = 10 V dc, 6,000 cycles.	
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 3			3 devices c = 0
Destructive physical analysis	2102		
Subgroup 4			
Thermal impedance, thermal resistance curves	3131	Each supplier shall submit their (typical) maximum design thermal impedance curves to the qualifying activity. In addition, the optimal test conditions and $Z_{\theta JX}$ limit shall be provided to the qualifying activity in the qualification report.	Sample size N/A
Subgroup 5			5 devices c = 0
Barometric pressure (2N3743, 2N3743U4, 2N4931, and 2N4931U4 only)	1001	V_{CBO} = 350 V, I_C = 10 nA, condition D, Pressure = 8 mm HG, normal mounting, t = 60 seconds minimum.	
Subgroup 6			3 devices
ESD	1020		
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B for devices $<$ 400 V.	



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 5. Derating for 2N3743 (TO-39).



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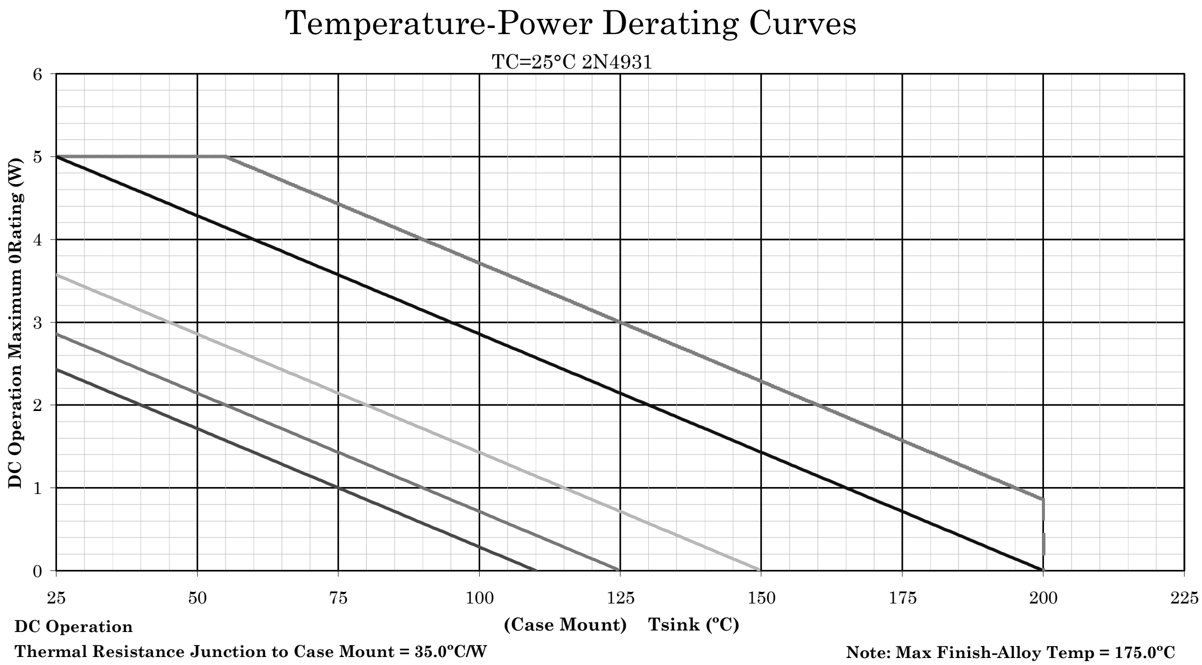
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 6. Derating for 2N4930 (TO-39).



NOTES:

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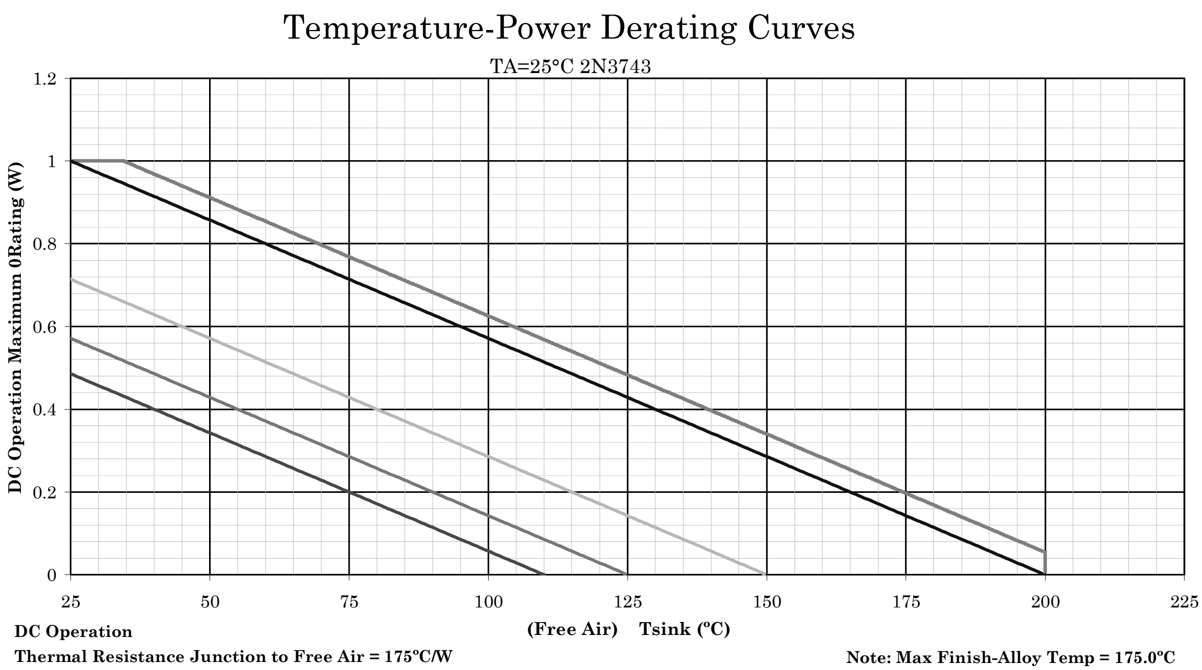
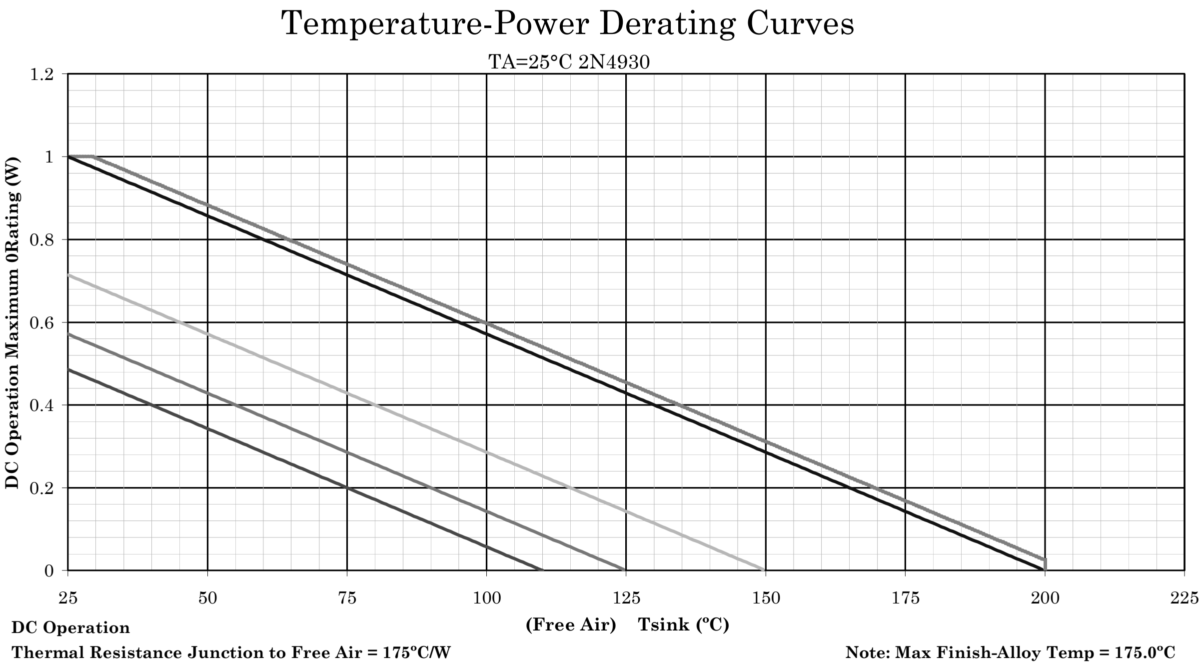
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 7. Derating for 2N4931 (TO-39).



NOTES:
1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 8. Derating for 2N3743 (TO-39).



NOTES:

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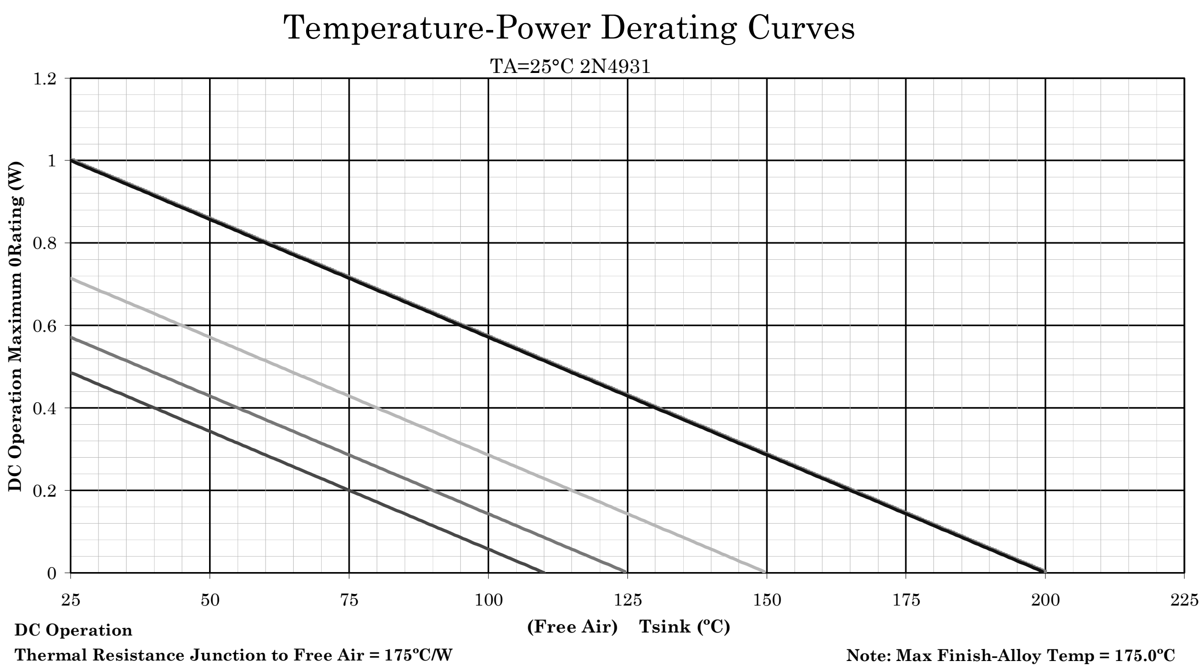
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 9. Derating for 2N4930 (TO-39).



NOTES:

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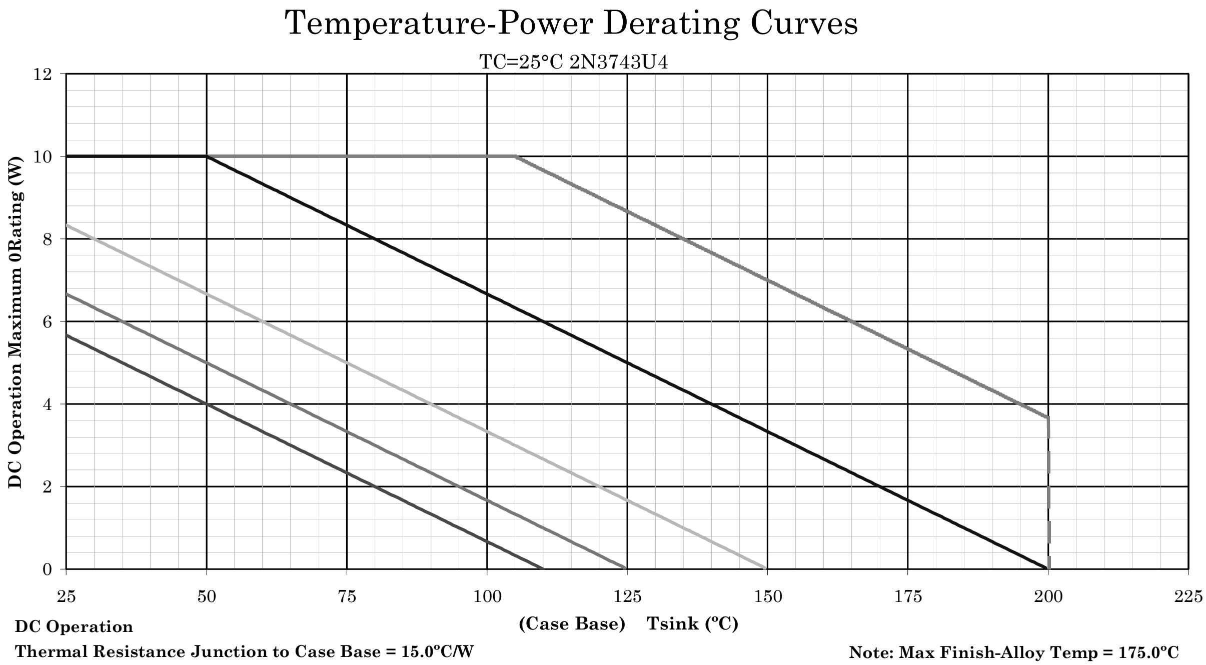
3. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 10. Derating for 2N4931 (TO-39).



NOTES:

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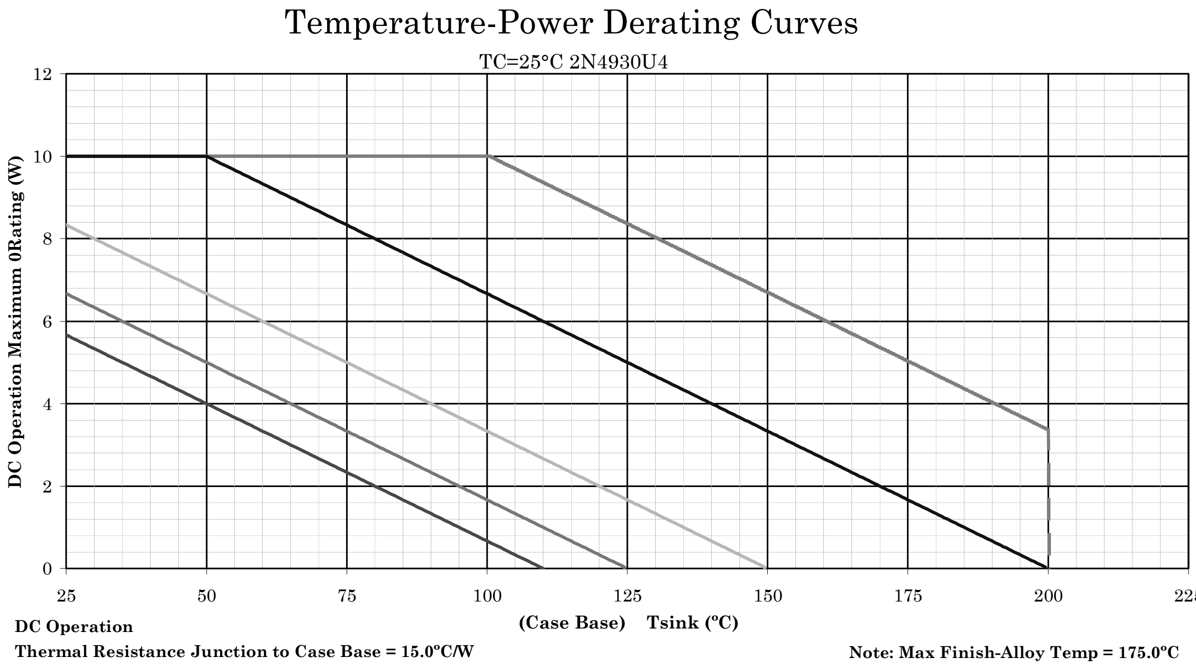
FIGURE 11. Derating for 2N3743U4.



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1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
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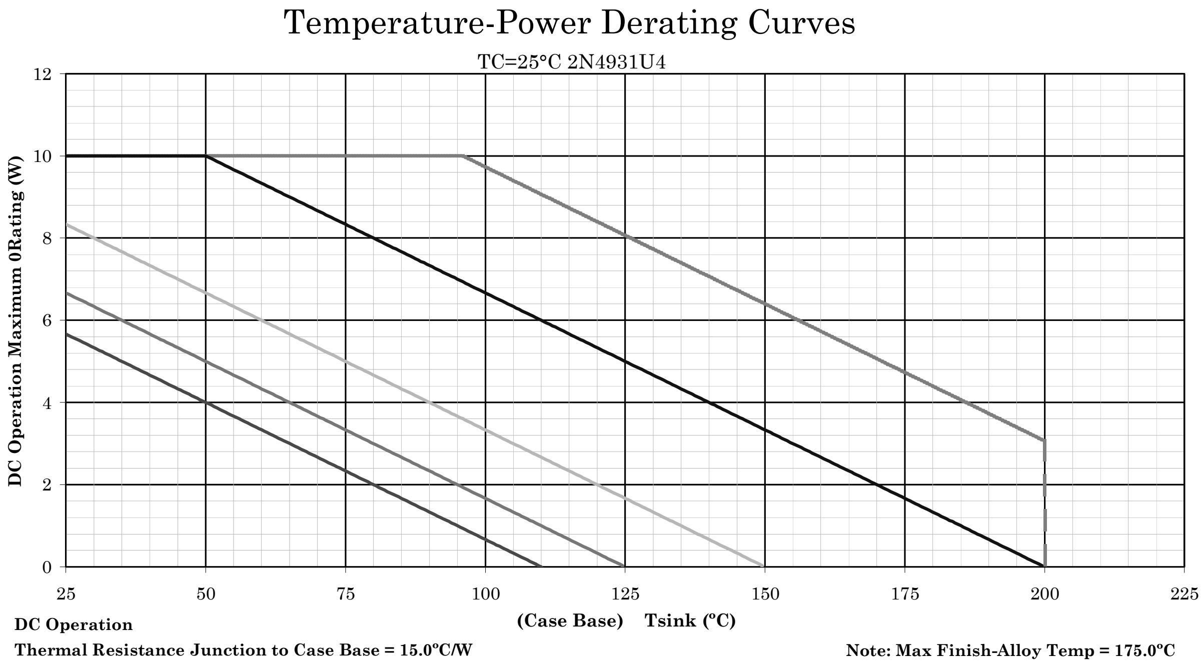
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 12. Derating for 2N4930U4.



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
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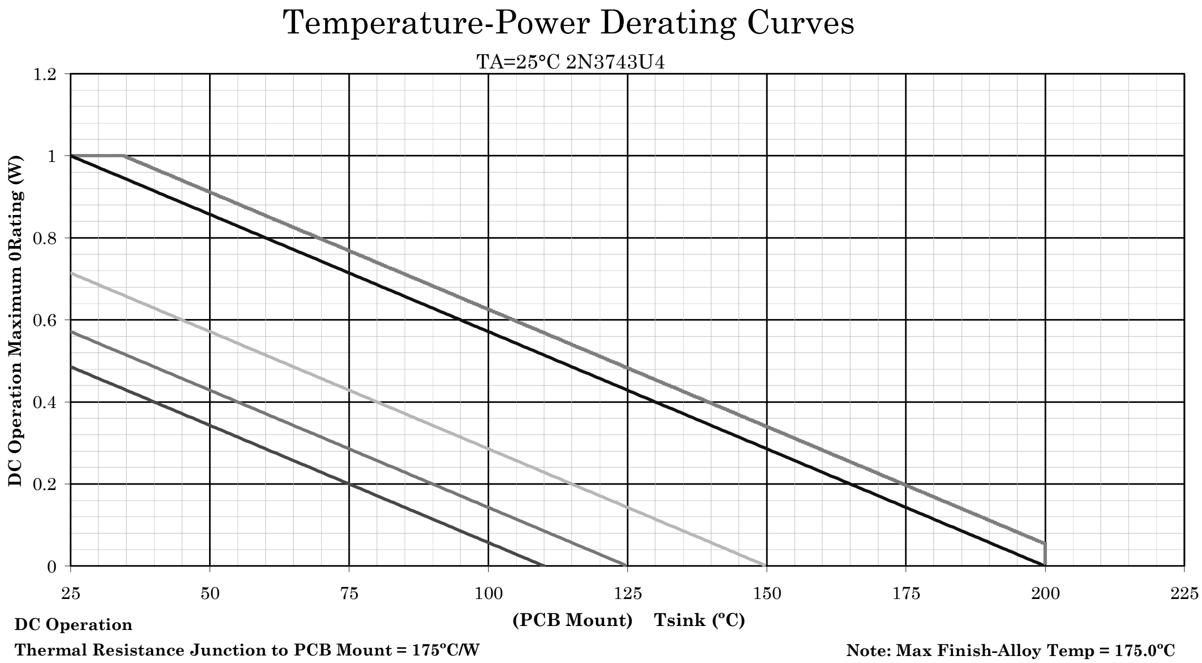
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

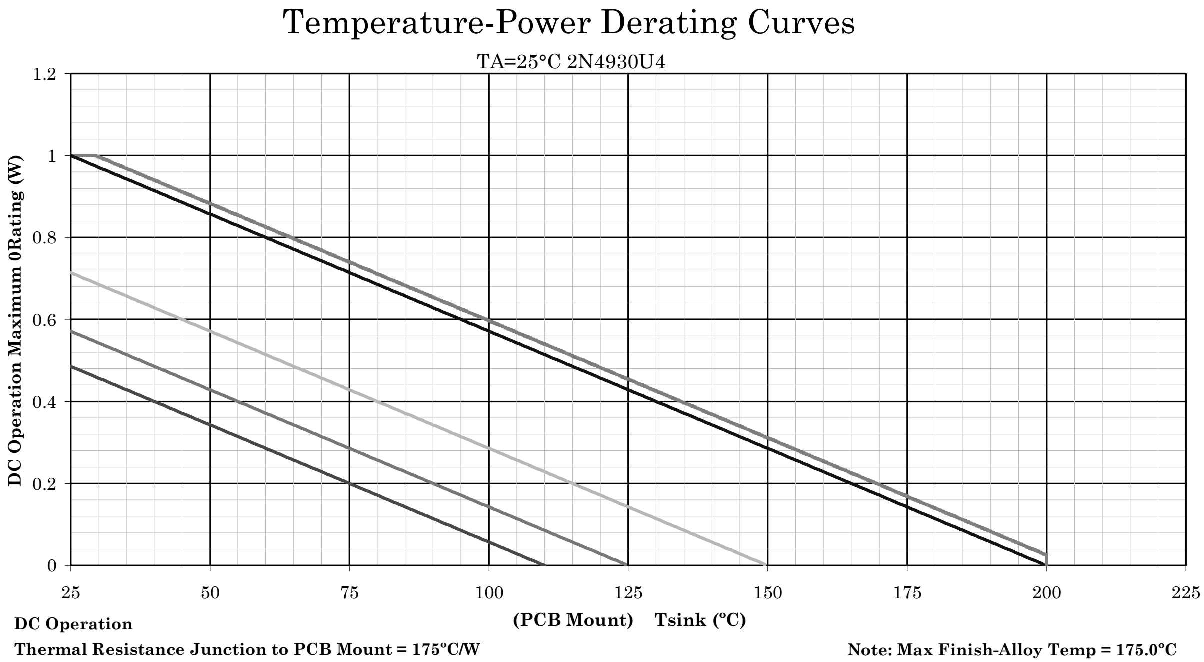
FIGURE 13. Derating for 2N4931U4.



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 14. Derating for 2N3743U4.



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
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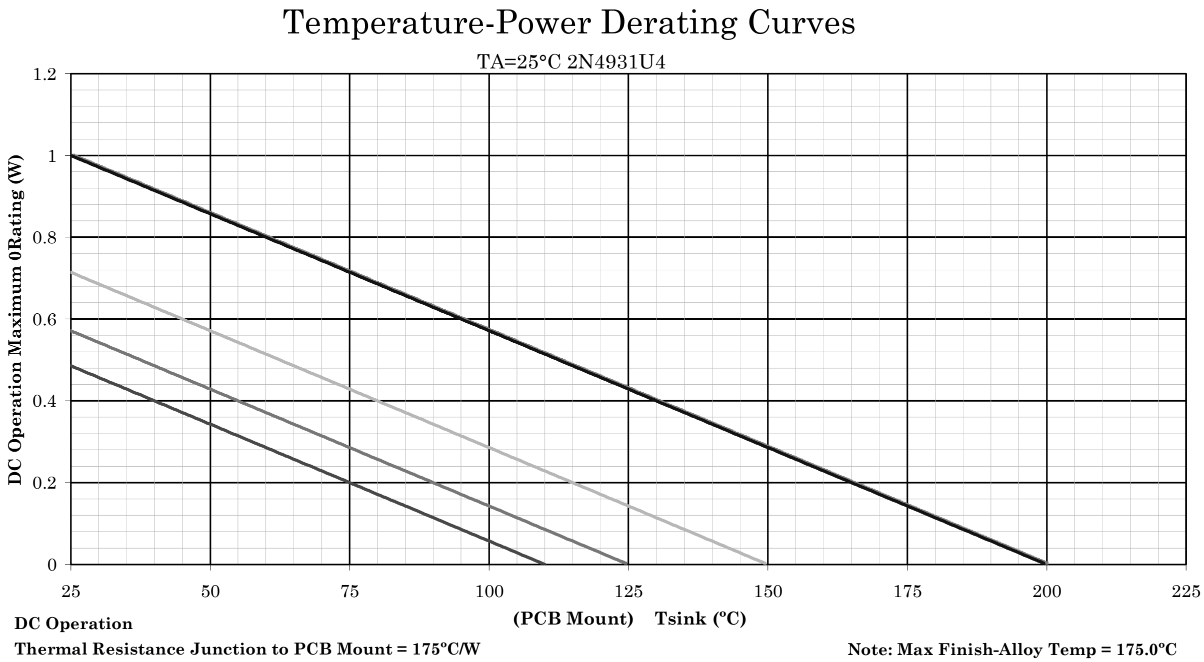
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 15. Derating for 2N4930U4.



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3.)
2. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
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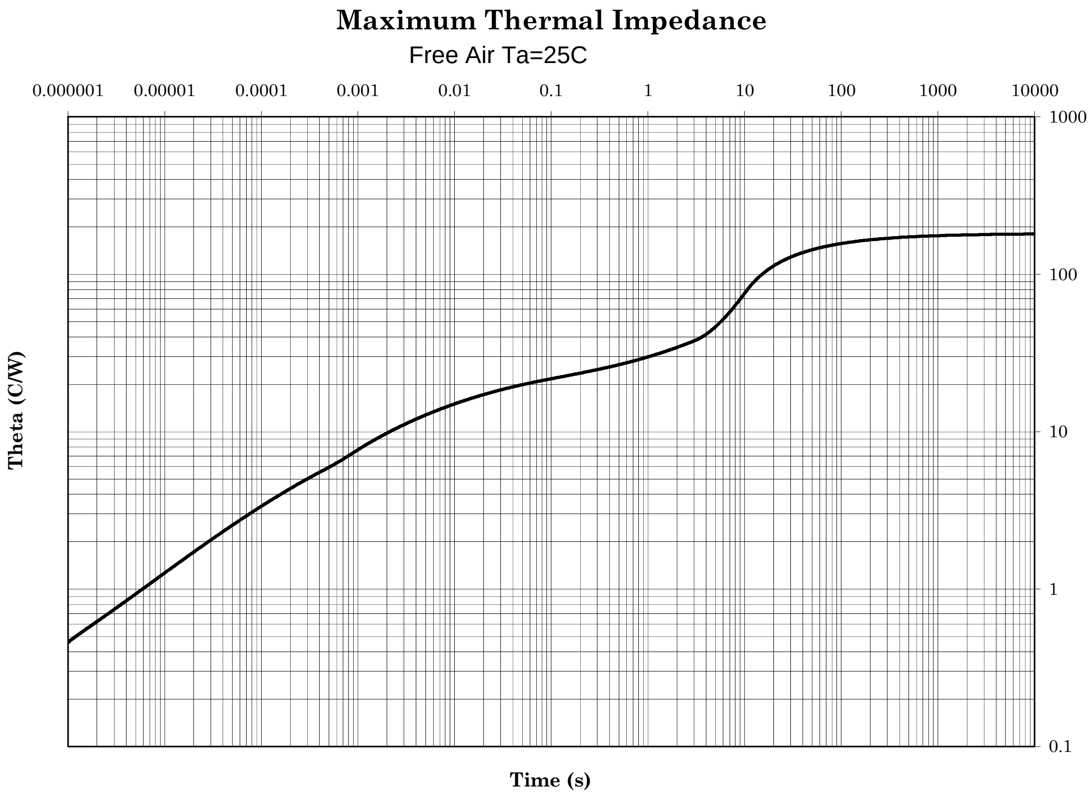
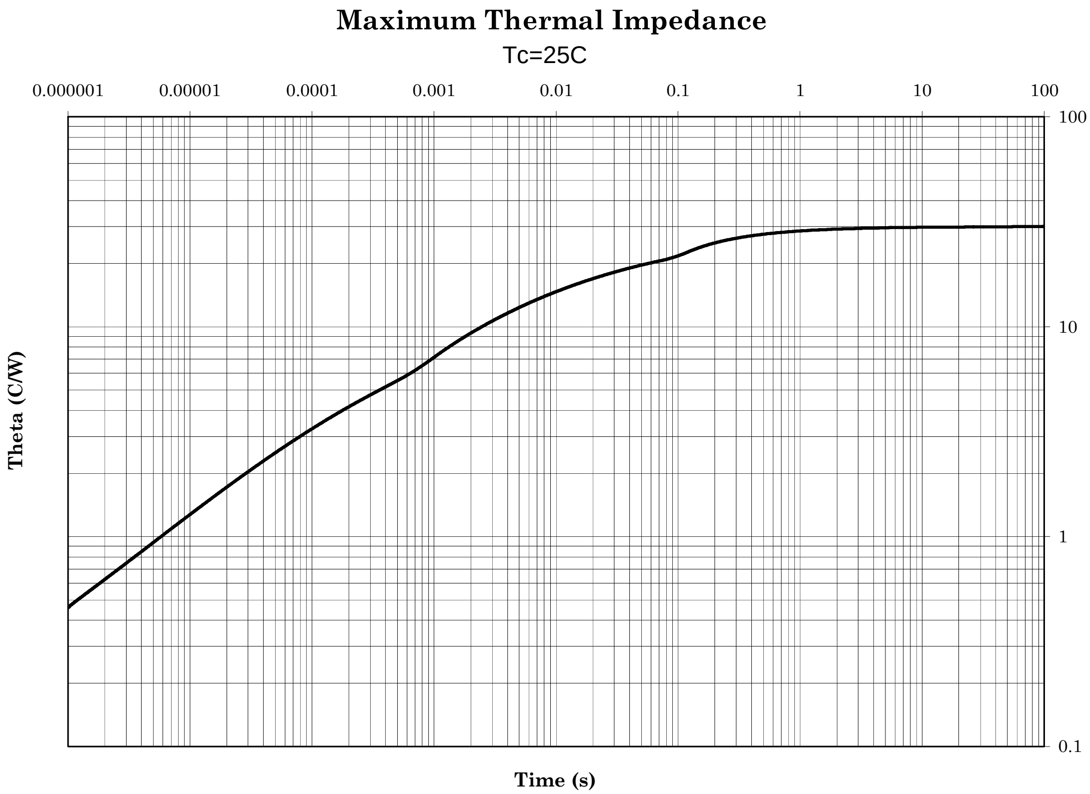
FIGURE 16. Derating for 2N4931U4.



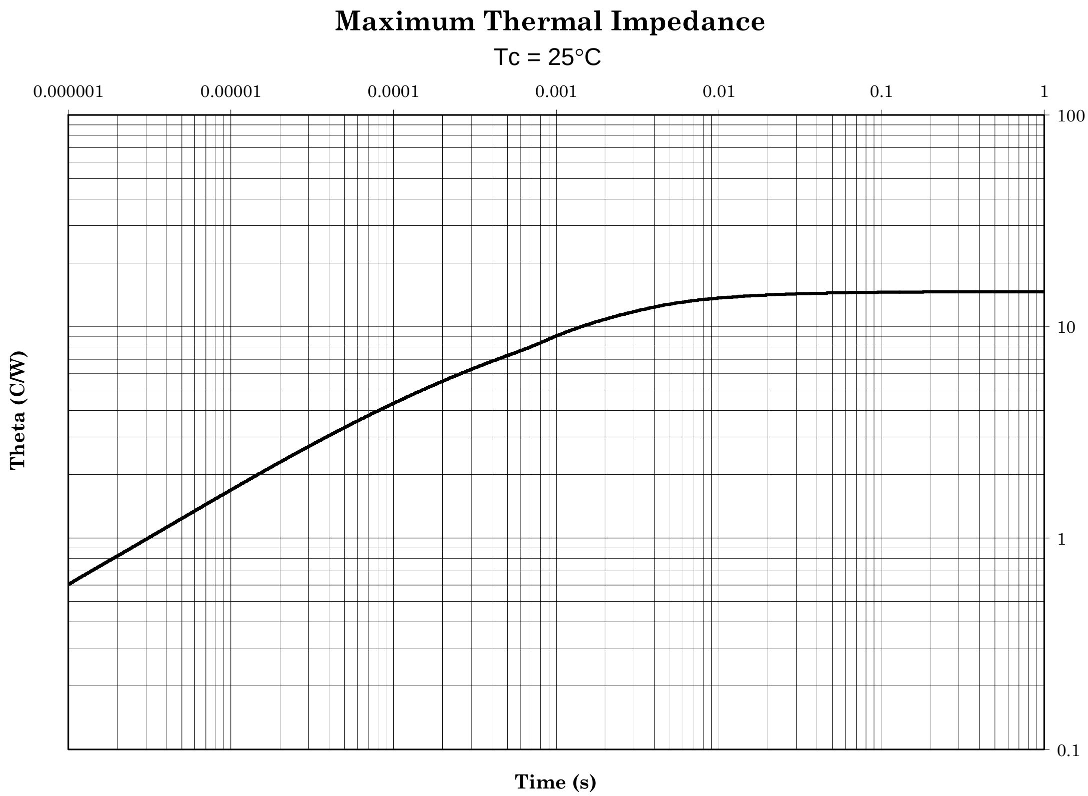
$R_{\theta JA}$ = 175°C

FIGURE 17. Thermal impedance for 2N3743, 2N4930, 2N4931(TO-39).



$R_{\theta JC} = 30°C$

FIGURE 18. Thermal impedance for 2N3743, 2N4930, 2N4931 (TO-39).



$R_{\theta JC}$ = 15°C

FIGURE 19. Thermal impedance for 2N3743U4, 2N4930U4, 2N4931U4 (U4).

5. PACKAGING

* 5.1. Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Points' packaging activity within the Military Service or Defense Agency, or within the Military Service's system Command. Packaging data retrieval is available from the managing Military Departments' or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. The lead finish as specified (see 3.4.1).

d. Product assurance level and type designation.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers' List (QML No. 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturers' PIN's are suitable as a substitute for the military PIN.

Preferred types Military PIN	Commercial PIN
2N3743	SUN1446H, SS4238H
2N4930	SUN1446H, SS5152H
2N4931	SUN1446H, ST1390H, ST147H

6.5 Suppliers of JANHC and JANKC die. The qualified die suppliers with the applicable letter version (example, JANHCA2N3743) will be identified on the qualified manufacturer's list.

JANC ordering information		
PIN	Manufacturers	
	33178	43611
2N3743	JANHCA2N3743, JANKCA2N3743	JANHCB2N3743, JANKCB2N3743
2N4930	JANHCA2N4930, JANKCA2N4930	JANHCB2N4930, JANKCB2N4930
2N4931	JANHCA2N4931, JANKCA2N4931	JANHCB2N4931, JANKCB2N4931

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2713)

Review activities:
Army - AR, AV, MI
Navy - AS, MC
Air Force – 19, 71

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://www.dodssp.daps.mil.